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[BUMP LAYOUT ON SILICON CHIP]

Abstract

A bump layout on the active region of a driver IC for increasing overall bump count. The layout fits IC packages that have a narrow and long body profile. Bumps are positioned close to the long side and central regions of the active region so that low marking pressure on the shorter sides of the package during chip-glass bondage is avoided. Dummy bumps may also be positioned close to the shorter sides of the package so that pressure distribution is optimized during chip-glass bondage.